

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Patent Application Serial No.:	10/824,069	)	Group Art Unit:	1792
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Filing Date:	April 13, 2004	)	Examiner:	Vinh, Lan
		)		
For:	Selectively Accelerated Plating of Metal Features	)	Docket No:	101.113
		)		
Inventors:	Drewery et al.	)	Confirmation No.:	7008
		)		
		)	Paper No.:	

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**RULE 132 DECLARATION OF STEVEN T. MAYER**

I, Steven T. Mayer, hereby declare:

1. I am a Director and Principal Engineer at Novellus Systems, Inc., working at the Novellus facility located at 11155 SW Leveton Drive, Tualatin, Oregon, 97062, where I am involved in conducting various research and development activities. These activities include developing techniques, processes and apparatuses for depositing metal during integrated circuit fabrication. As such, I have the knowledge of one skilled in the art of deposition, removal, and treatment of thin films using liquid chemical reactions. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

2. My formal education includes a Ph.D. from the University of California at Berkeley. I have worked for ten years as a Technologist, Process Development Engineer and Principal Engineer at Novellus Systems, Inc., five years as Chief Technical Officer at PolyStor Corporation, and four years at Lawrence Livermore National Laboratories as Senior Staff Scientist. I have authored about 20 published papers on the subject of integrated circuit process engineering, and many more in the area of electrochemical engineering. I am a named inventor in over 50 issued patents, the majority of them in the field of integrated circuits and am discussed in Marque's "Who's Who in America".

3. I am one of the inventors and Novellus Systems, Inc. is the assignee of the above-designated patent application (hereinafter "the present application").

**Serial No. 10/824,069**  
**Declaration of Steven T. Mayer**  
**January 2008**

4. As a person skilled in the art of deposition, removal, and treatment of thin films using liquid chemical reactions during integrated circuit fabrication, I submit this Declaration to present to the Examiner, in an authenticated manner, facts concerning the teachings of the "Specification" in the present application, the references cited in the Office Action mailed November 2, 2007, and their relevance to claims 46 -- 91 of the present application, particularly to independent claims 46 and 58.

5. I have read the currently pending claims 46 -- 91 of the application, the Office Action, and the references cited by the Examiner, in particular: Matsuda et al., U.S. Patent Application Publication US 2004/0226827, published November 18, 2004 (hereinafter "Matsuda et al."); and Nakamura et al., U.S. Patent Application Publication US 2001/0013472, published August 16, 2001 (hereinafter "Nakamura et al.").

6. The difference in copper height/thickness in Matsuda et al. is undesirable and its reduction and elimination are a goal of Matsuda et al., as discussed in Matsuda et al. in Example 1, para. [0109-0110], referring to FIG. 5C.

7. Matsuda et al. teach using CMP (chemical mechanical polishing) to remove plated copper film 31, seed layer 30 and barrier layer 29 (FIG. 5C) from the entire surface down to the top surface of insulating film 26 (FIG. 5D). Matsuda et al., para. [0112]. CMP is not an isotropic technique. It is used generally in the art to planarize an un-smooth surface, that is, to make it smooth, as depicted in FIG. 5D of Matsuda et al.

8. In contrast, an isotropic metal removal technique, as claimed in new claims 46 and 58, removes the same material at substantially the same rate from all locations of a surface, thereby substantially maintaining the original general shape of the surface (even if lowering it uniformly), as depicted in FIG. 10. As a result of isotropic metal removal, plated copper protrudes above the resist layer (after removing metal from the field region) in preferred embodiments in accordance with claims 46 and 58. In contrast, in Matsuda et al., CMP planarizes the surface and the plated metal does not protrude above insulating film 26. For example, compare FIG. 5D of Matsuda et al. with FIG. 10 of the present application.

**Serial No. 10/824,069**  
**Declaration of Steven T. Mayer**  
**January 2008**

9. Matsuda et al. disclose a difference of only 0.4  $\mu\text{m}$  (FIG. 6, para. [0114, 0116]) and 0.2  $\mu\text{m}$  (FIG. 7, para. [0122]).

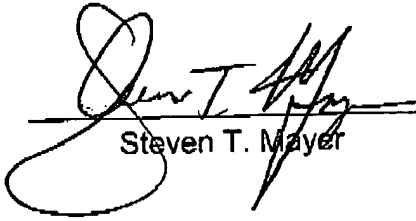
10. At page 3, para. [0051], Nakamura et al. teach using a copper-etching solution to remove plating promoter from the surface of copper film 21, which is essentially a copper seed layer. The etching solution is neither isotropic nor used to remove copper/metal from the field region after plating copper/depositing metal in the acceleration region and field region.

11. At page 4, para. [0060], Nakamura et al. teach patterning by etching, which as a practical matter, can only be accomplished by masking the surface prior to etching. Furthermore, the method could not be isotropic to achieve the selective metal removal as shown between Figs. 4 and 5 of Nakamura et al.

12. Thus, the combination of the etching in Nakamura et al. with the method of Matsuda et al. does not teach all the claim limitations of the currently pending claims. Furthermore, Matsuda et al. need a planarization technique, such as CMP, to planarize their substrate. The etching solution of Nakamura et al. could not perform this function. Thus, there is no motivation or suggestion in the references or in the art to combine the references as suggested by the Examiner, and there would be no expectation of success.

13. I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and that such willful false statements may jeopardize the validity of the present application or any patent issued thereon.

1/28/2008  
Date

  
Steven T. Mayer

Serial No. 10/824,069  
Declaration of Steven T. Mayer  
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